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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 6

Complete if Known

Application Number	10/005,105
Filing Date	December 3, 2001
First Named Inventor	Paul C. Kocher
Art Unit	2132
Examiner Name	Abdulhakim Nobahar
Attorney Docket Number	44424162-8721

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (If known)			
	V70	US 2,632,058 B1	03-17-1953	Gray	
	V71	US 2,733,432 B1	01-31-1956	Breckman	
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		Number-Kind Code ² (if known)			
	V95	US 5,859,548 B1	01-12-1999	Kong	
	V96	US 5,905,399 B1	05-18-1999	Bosnyak et al.	
	V97	US 5,917,754 B1	06-29-1999	Pathak et al.	
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		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
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				Group Art Unit	2132
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Sheet	3	of	6	Attorney Docket No.	44424162-8721
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	V107	DAVIES & PRICE, Security for Computer Networks: An Introduction to Data Security in Teleprocessing and Electronic Funds Transfer, John Wiley & Sons, New York, NY, 2nd Ed., 1989, 377 pages (entire book).			
	V108	Defendant VISA International Service Association's Final Invalidity Contentions for U.S. Patent No. 6,304,658 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.			
	V109	Defendant VISA International Service Association's Final Invalidity Contentions for U.S. Patent No. 6,381,699 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.			
	V110	Defendant VISA International Service Association's Final Invalidity Contentions for U.S. Patent No. 6,510,518 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.			
	V111	Defendant VISA International Service Association's Final Invalidity Contentions for U.S. Patent No. 6,654,884 Pursuant to Patent L.R. 3-6(b), February 8, 2008, Case No. C04-04143 JW(HRL), U.S. District Court, Northern District of California, San Jose Division.			
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	V113	BACK, Adam, "non-interactive forward secrecy", posting to Cypherpunks.Venona.com message board, September 6, 1996. http://cypherpunks.venona.com/date/1996/09/msg00561.html			
	V114	DRAPER, Don et al., "Circuit Techniques in a 266-MHz MMX-Enabled Processor", <i>IEEE J. Solid State-Circuits</i> , pp. 1650-1664, November 1997.			
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	V115	EBERLE, Hans & THACKER, Charles P., "A 1 GBIT/Second GAAS DES Chip", <u>Proceedings of the 1992 IEEE Custom Integrated Circuits Conference</u> , May 3-6, 1992.			
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	V119	HOUGH, Charles et al., "New Approaches for On-Chip Power Switching Noise Reduction", <u>Proceedings of the IEEE 1995 Custom Integrated Circuits Conference</u> , May 1-4, 1995, pp 133 - 136.			
	V120	IVEY, Peter A. et al, "A Single-Chip Public Key Encryption Subsystem", <u>IEEE J. Solid-State Circuits</u> , 24(4):1071-1075, August 1989.			
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	V122	JARECKI, Stanislaw, "Proactive Secret Sharing and Public Key Cryptosystems", thesis, Massachusetts Institute of Technology, September 1995, Cambridge, MA.			
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	V123	KARLSSON, Magnus et al., "Implementation of bit-serial adders using robust differential logic," <u>Proc. IEEE Nordic Event in ASIC Design Conf.</u> , NORCHIP'97, Tallin, Estonia, Nov 10-11, 1997.			
	V124	LARSSON, Patrik, " <u>di/dt Noise in CMOS Integrated Circuits</u> ", <u>Analog Integrated Circuits and Signal Processing</u> , 14:113-129, Kluwer Academic Publishers, Boston, MA, 1997.			
	V125	LIN, Mao-Chao, "Constant Weight Codes for Correcting Symmetric Errors and Detecting Unidirectional Errors", <u>IEEE Transactions on Computers</u> , 42(11): 1294-1302, November 1993.			
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	V131	OKLOBDZIJA, Vojin G., "Differential and Pass-Transistor CMOS Logic for High-Performance Systems", <u>Proc. 21st International Conference on Microelectronics (MIEL'97)</u> , 2:803-810, Nis, Yugoslavia, September 14-17, 1997.			
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	V132	SCHETTLER, Helmut et al., "A CMOS Mainframe Processor with 0.5-μm Channel Length", <u>IEEE Journal of Solid-State Circuits</u> , 25(5):1166-1177, October 1990.			
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	V136	TALLINI, Luca G. & BOSE, Bella, "Design of Balanced and Constant Weight Codes for VLSI Systems", <u>IEEE Transactions on Computers</u> , 47(5):556-572, May 1998.			
	V137	TEXAS INSTRUMENTS, SN54LS138, SN54S138, SN74LS138, SN74S138A 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS, Texas Instruments, Dallas, Texas, revised March 1988.			
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	V139	WILLIAMS, Ted E. & HOROWITZ, Mark, "Bipolar Circuit Elements Providing Self-Completion-Indication", <u>IEEE Journal of Solid-State Circuits</u> , 25(1):309-312, February 1990.			
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